Design and characterization of a clock distribution circuit for QCA

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Abstract

In this paper we introduce and characterize a novel circuit design for low power clock distribution for quantum-dot cellular automata (QCA) systems. The characterization of the clocking circuitry includes an evaluation of: the coupling capacitances among the wires and with the ground plane; the dissipative effects of the wires and the substrate; the phase shift between neighboring wires; and the number of wires driven by the same clock line. The electrical characteristics of the clocking circuitry are a function of the chosen design parameters. The clock tree is initially modeled as an RC circuit. A resonant RLC circuit is then proposed, and its power dissipation performance is compared to an RC circuit as a function of the quality factor Q of the resonating circuit. It is shown that this approach can greatly reduce the power dissipated in the clocking layer of a QCA circuit.

I. Introduction

Among the innovative technologies that have been proposed to overcome the limitations of "end of the roadmap" CMOS, Quantum-dot Cellular Automata (QCA) shows features that are very promising to achieve both high computational throughput and low power dissipation. The QCA computational paradigm [1] [2] [3] on one hand introduces highly pipelined architectures with extremely high speeds (in the order of THz) while on the other hand radically departs from switch based CMOS, avoiding the movement of charge from $V_{\rm dd}$ to Ground and the consequent energy dissipation. An operating single cell [4] and a functional logic gate have been demonstrated [5] using metal dot implementations at cryogenic temperatures. Moreover, recent advances in fabrication of molecular scale QCA cells suggest the realizability of QCA cells a few nanometers on a side that would allow room temperature operation.

In addition to having great promise for being small, high speed devices, it has been shown that QCA has great potential for low power operation. The reversible computation paradigm is particularly well suited to QCA since

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Timler showed that in a clocked, information preserving system, the energy dissipation of the QCA circuit can be much lower than $k_{\mathrm{B}}T\ln 2$ [6].

Details on reversible QCA design strategies are out of the scope of this paper, however very power efficient QCA circuits will be of little utility without a clock distribution strategy of equal or superior power efficiency.

The goal of this paper is to address the characterization of the clock distribution circuits for QCA and to propose low power design solutions. While there is a substantial body of work concerning the design of QCA circuits, little has been done about the design and characterization of the clock distribution circuits. There are many unanswered questions about the power performance of the clock circuits. This work is the first step toward answering these questions.

This paper is organized as follows: section 2 introduces the clock distribution strategies for QCA and section 3 provides a model of the capacitances of the clocking circuitry. Section 4 introduces a possible improvement over a simple RC circuit by including a resonating RLC circuit and section 5 evaluates the power performances of the resonating clocking distribution under different parameters. Finally section 6 draws the conclusions.

II. Overview on clock distribution circuit for QCA

In the early proof of concept [7] work, the clock was explicitly delivered to every cell through metal wires. This was sufficient for the goals of the experiments, but it has some obvious shortcomings and prohibits large scale integration. In order to overcome these and to facilitate a shift toward molecular QCA, a clocking scheme was envisioned that would use a sequence of metal wires buried beneath the QCA layer that would generate an E-field that would control the tunneling within the QCA layer [8]. By variably controlling the strength of the field at different points, directionality can be imposed on the QCA circuit. In the typical scheme the wires are divided into four groups, and each wire is assigned a phased sinusoidal voltage source $V(t) = V\sin(2\pi f_0 t + \phi_i)$. The phases of the wires are $\phi_i = i \cdot \frac{\pi}{2}(i = 0, 1, 2, 3)$. Note that at least three phases are needed to provide directionality to the flow of information on the QCA layer.

Figure 1 shows a cartoon view of a possible implementation of the four phased clock distribution for QCA. The wires are actually on the top of the QCA layer to take advantage of the typical planar process for the metalization. A ground plane is found on the other side of the QCA layer from the clocking wires in order to terminate the E-field lines. Four wires ($\Phi_1, \Phi_2, \Phi_3, \Phi_4$) carry the four phase shifted signals. The actual distribution on the QCA layer is obtained through smaller wires branched out from the main carriers.

III. Capacitive coupling

The overall capacitive effects on the clocking wires can be considered as the sum of two main contributions:

$$C_{\mathrm{tot}} = C_{\mathrm{W}} + C_{\mathrm{L}}$$

where C_{W} represents the coupling with neighboring wires and C_{L} represents the coupling with the ground plane. In the following subsections we analyze in detail these two contributions.

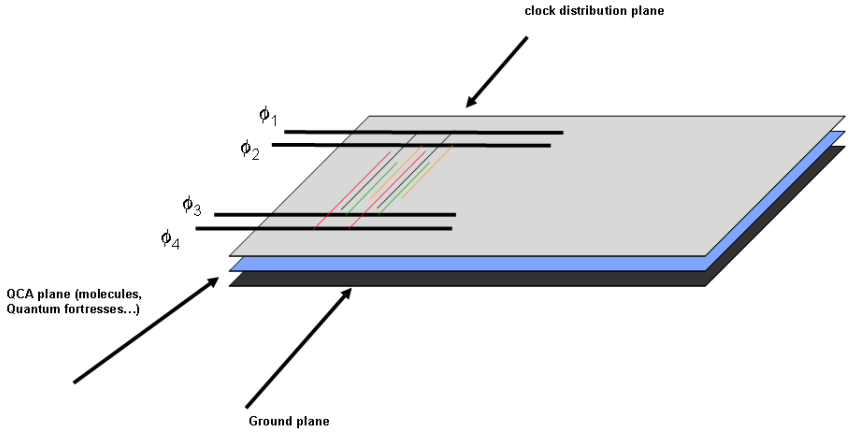

Fig. 1. Possible clock distribution circuitry for QCA

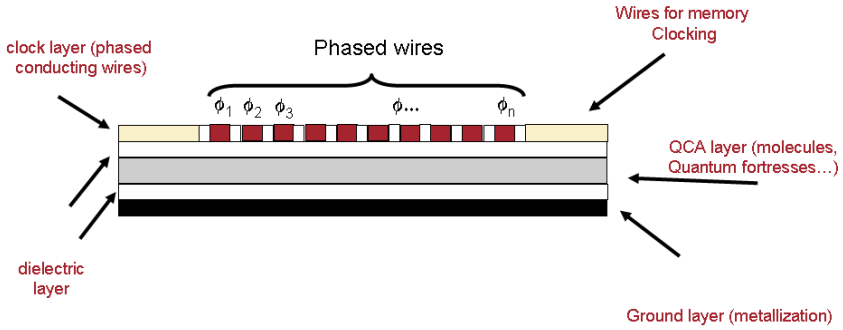

Fig. 2. Cross Section of a generic QCA implementation

A. Capacitive coupling with the neighboring wires

The clock wires experience a capacitive coupling with their neighbors. For a generic wire, the strongest coupling occurs with the two closest neighbors. The capacitance model between wires (that is usually called $C_{\rm m}$) is typically obtained in VLSI by solving Green's function with a multipole expansion (as in the FastCap software [9]), by using a finite difference method to solve the Poisson equation (1Poisson [10]), or by using finite elements (FIERCE [11]). Since this work is the first one addressing the problem of QCA clocking circuit design, we make the simplifying assumption that the value of the capacitance is obtained from the simple plane capacitor formula

$$C_{\rm m} = \epsilon_0 \epsilon_{\rm r}^{\rm w} \cdot \frac{A_{\rm w}}{d_{\rm w}}$$

where $d_{\rm w}$ is the distance between two neighbor wires, $A_{\rm w}$ is the area of the wire exposed to the neighbors and $\epsilon_{\rm r}^{\rm w}$ is relative permittivity of the dielectric between the wires. Future work can address the refinement of the model.

In addition, there is an effect similar to what happens in VLSI when the wires of a bus are affected by crosstalk [12], the time varying signal on the two neighboring wires affects the total charge Q that needs to be provided

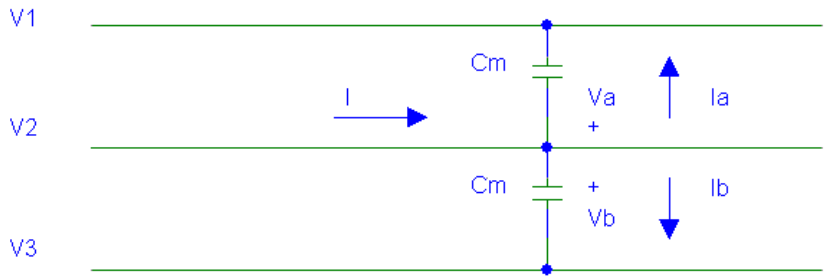

Fig. 3. Parasitic coupling with neighbor wires

to the target wire to obtain a certain value of V on it. This effect can be modeled with a k multiplicative factor applied to C_{m}.

Consider a wire coupled with its two neighbors through the capacitance C_{m} as shown in Figure 3. The equivalent capacitance seen on the middle wire can be calculated as follows:

$$\begin{aligned} V_1(t) &= \sin(\omega t - \phi) \\ V_2(t) &= \sin(\omega t) \\ V_3(t) &= \sin(\omega t + \phi) \end{aligned}$$

where ϕ represents the phase shift between neighboring wires.

Further,

$$V_a(t) = V_2(t) - V_3(t) = -2\sin\frac{\phi}{2} \cdot \cos\left(\omega t + \frac{\phi}{2}\right)$$

$$V_b(t) = V_2(t) - V_1(t) = 2\sin\frac{\phi}{2} \cdot \cos\left(\omega t - \frac{\phi}{2}\right)$$

from the definition of capacitance:

$$I_b(t) = C_m \frac{dV_b(t)}{dt}$$

$$I_a(t) = C_m \frac{dV_a(t)}{dt}$$

and from the Kirkhoff's Law

$$I(t) = I_a(t) + I_b(t) = C_m \left(\frac{dV_a}{dt} + \frac{dV_b}{dt}\right)$$

being:

$$\frac{dV_a}{dt} = 2\omega \sin\frac{\phi}{2} \sin\left(\omega t + \frac{\phi}{2}\right)$$

$$\frac{dV_b}{dt} = -2\omega \sin\frac{\phi}{2} \sin\left(\omega t - \frac{\phi}{2}\right)$$

Therefore the current is:

$$\begin{aligned} I(t) &= 2C_m\omega \sin\frac{\phi}{2}\left[\sin\left(\omega t+\frac{\phi}{2}\right)-\sin\left(\omega t-\frac{\phi}{2}\right)\right] \\ &= 4C_m\omega \sin\frac{\phi}{2}\left[\cos(\omega t)\sin\left(\frac{\phi}{2}\right)\right] \end{aligned}$$

The capacitance seen on the middle wire is therefore (from the definition of capacitance)

$$C_{\mathrm{W}} = \frac{I(t)}{\mathrm{d}V_2(t)/\mathrm{d}t}$$

where

$$\frac{\mathrm{d}V_2(t)}{\mathrm{d}t} = \omega\cos(\omega t)$$

and therefore finally:

$$C_{\mathrm{W}} = k\cdot C_{\mathrm{m}} = 4\sin^2\frac{\phi}{2}\cdot C_{\mathrm{m}}$$

B. Capacitive coupling with the ground plane and dissipative effects

As shown in Figure 2, the QCA layer is sandwiched between the clocking wires and the ground plane. The capacitance through the QCA layer depends on the relative permittivity of the chosen material to implement the QCA circuits and on its vertical size. Similar to what was seen for C_{W}, a simplifying assumption is made to model C_{L} as:

$$C_{\mathrm{L}} = \epsilon_0\epsilon_r^q\cdot\frac{A_q}{d_q}$$

where d_q is the distance between the wire and the ground plane, A_q is the area of the wire facing the QCA layer and ϵ_r^q is relative permittivity of the QCA layer.

IV. Resonant RLC circuit for low power clock distribution

Consider a simple RC circuit (see fig 4) as the model of the clock distribution where R_{W} represents the overall resistance of the clocking wire ($R_{\mathrm{W}} = R_{\mathrm{W1}} + R_{\mathrm{W2}}$, where R_{W1} is the resistance of the distribution wire with larger cross-section, R_{W2} is the resistance of the clocking wire with smaller cross-section), C_W represents its capacitance with its two neighboring wires, and C_{L} and R_{L} represent the capacitance and the dissipative effect with the ground plane through the dielectric composing the QCA layer. The total capacitance is $C_{\mathrm{tot}} = C_W + C_{\mathrm{L}}$, and the power dissipated per clock period can be calculated as follows.

From the definition of voltage as the energy per unit charge, the energy stored on the ideal capacitor should be $QV = C_{\mathrm{tot}}V^2$ since all the work done on the charge in moving it from one plate to the other would appear as

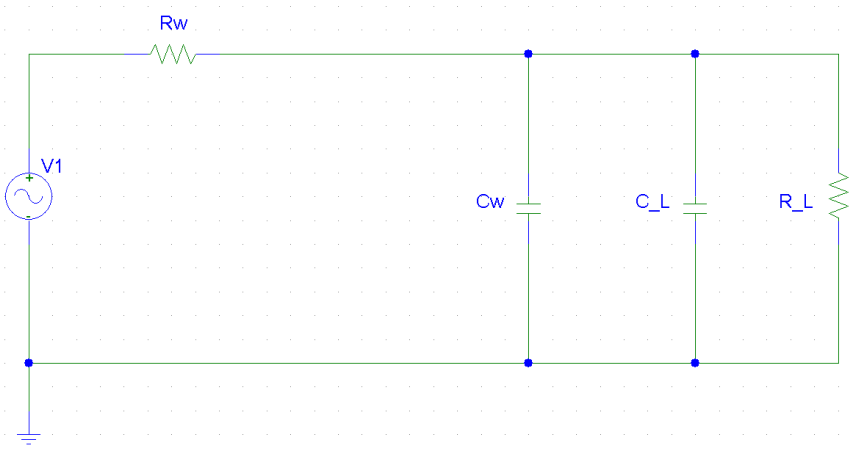

Fig. 4. Model of Clocking with an RC circuit

energy stored. However, since the work done to put a $\mathrm{d}q$ charge at a potential V is $\mathrm{d}U = V\mathrm{d}q$, the total energy to put Q charge on the capacitor is

$$U = \int_0^Q V\mathrm{d}q = \int_0^Q \frac{q}{C_{\mathrm{tot}}}\mathrm{d}q = \frac{Q^2}{2C_{\mathrm{tot}}} = \frac{C_{\mathrm{tot}}V^2}{2}$$

This expression shows that just half of the $QV = C_{\mathrm{tot}}V^2$ work appears as energy stored in the capacitor. For a finite value of R_{W} and assuming that R_{L} is negligible compared to C_{L}, half of the energy supplied by the power supply for charging the capacitor is dissipated as heat in the resistor, regardless of the size of the resistor. Considering voltage swing on the supply from 0 to V, then, the energy dissipated on R_{W} in the charge and discharge of the capacitor C_{tot} occurring in a period is $C_{\mathrm{tot}}V^2$. Therefore, for a frequency of operation f_0, the power dissipated on the clocking distribution circuit is:

$$P_{\mathrm{RC}} = C_{\mathrm{tot}}V^2 f_0 \tag{1}$$

Note that this analysis is valid for an abrupt switch of the current on the voltage source (square wave) it could be demonstrated that if a sinusoidal voltage source is considered then the previous equation should be multiplied by a factor ≤ 1 [13]. A detailed analysis of the adiabaticity of the voltage supply waveform will not be analyzed in the following as it does not affect substantially the results of the analysis.

To reduce the power dissipation the distribution of the clock could be done through a resonant parallel RLC circuit. A resonating circuit has a very limited current drain from the source at its resonating frequency. This has been studied for low power clock distribution in conventional VLSI [14] [15]. It is useful to compare the power dissipation of the RC and RLC circuits. We will show that if the resonant circuit has a good quality (measured by the Q factor) the introduction of the resonant tank improves dramatically the power performances.

Consider the RLC circuit in figure IV. L_{W} represents the inductor introduced to generate the resonant circuit. As before, the total capacitance is $C_{\mathrm{tot}} = C_W + C_{\mathrm{L}}$. The relation between L_{W} and C_{tot} to obtain resonance is

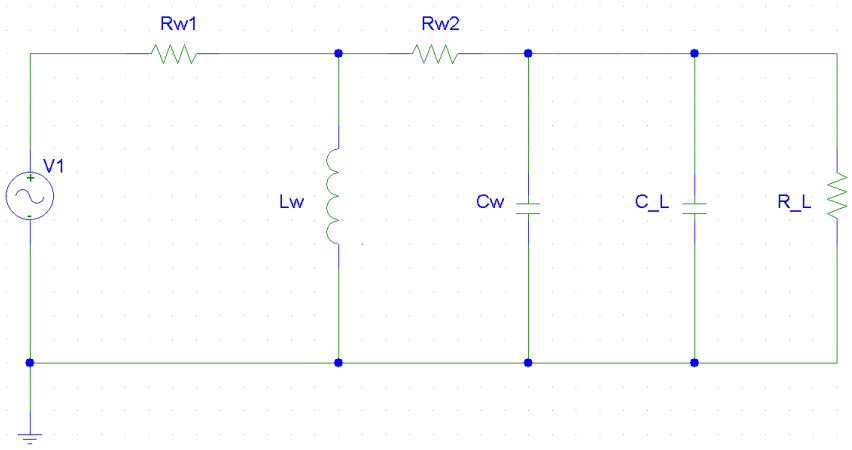

Fig. 5. Model of Clocking with an RLC resonating circuit

$2\pi f_0 L_{\mathrm{W}} = 1/(2\pi f_0 C_{\mathrm{tot}})$. Therefore, the resonant frequency can be obtained by:

$$f_0 = \frac{1}{2\pi\sqrt{L_{\mathrm{W}} C_{\mathrm{tot}}}} \tag{2}$$

L_{W} can be chosen to tune the value of the parasitic capacitances C_{tot}. Since at f_0 the reactive loads cancel each other, the current absorbed from the voltage supply flows only through the resistive load. Therefore the power dissipated at resonance is

$$P_{\mathrm{RLC}} = \frac{V^2}{2R_{\mathrm{tot}}} \tag{3}$$

where $R_{\mathrm{tot}} = R_{\mathrm{W1}} + R_{\mathrm{W2}} + R_{\mathrm{L}}$. To compare this result with the previous for RC in eq. 1 (similar to [14]) we introduce the definition of quality factor Q as:

$$Q = 2\pi f_0 \cdot \frac{Maximum\ Energy\ Stored}{Average\ Power\ Dissipation} \tag{4}$$

The maximum energy stored in the circuit is the amount of energy resonating between C_{tot} and L_{W} which can be expressed as the maximum amount of energy on the capacitance: $C_{\mathrm{tot}}V^2/2$. As shown above average power at resonance is $P_{\mathrm{RLC}} = V^2/2R_{\mathrm{tot}}$, therefore

$$\begin{aligned} Q &= 2\pi f_0 \cdot \frac{C_{\mathrm{tot}}V^2/2}{V^2/2R_{\mathrm{tot}}} \\ &= 2\pi f_0 \cdot R_{\mathrm{tot}} C_{\mathrm{tot}} \end{aligned} \tag{5}$$

From 6 and 3

$$P_{\mathrm{RLC}} = \frac{\pi C_{\mathrm{tot}} f_0 V^2}{Q}$$

The ratio between P_{RLC} and P_{RC} is therefore:

$$\frac{P_{\mathrm{RLC}}}{P_{\mathrm{RC}}} = \frac{\pi C_{\mathrm{tot}} V^2 f_0}{Q} \cdot \frac{1}{C_{\mathrm{tot}} V^2 f_0} = \frac{\pi}{Q} \tag{6}$$

Therefore, if $Q \geq \pi$ the RLC resonating circuit is dissipating less power than the RC.

A. *Parallel load effect*

Previously we considered that the voltage supply is connected to a single clocking wire, however, for real clocking of QCA circuits, the same voltage supply will most likely be connected to several (n) parallel clocking wires as shown in Figure 1. In this section we will introduce n as a parameter for the evaluation of the quality of the resonator. The introduction of n parallel loads will obviously affect both R_{tot} and C_{tot} yielding new values of $R'_{\mathrm{tot}} = R_{\mathrm{W1}} + \frac{R_{\mathrm{W2}}}{n} + \frac{R_{\mathrm{L}}}{n}$ and $C'_{\mathrm{tot}} = n \cdot C_{\mathrm{L}}$.

The parallel effect of the load equally effects C_{L} and R_{L}. The partition of current on them, then, remains the same. Therefore, the equation (1) for the RC circuit with n parallel wires is only slightly modified to:

$$P'_{\mathrm{RC}} \geq n \cdot C_{\mathrm{tot}} V^2 f_0$$

whereas for the resonant RLC circuit we have:

$$P'_{\mathrm{RLC}} = \frac{V^2}{2R'_{\mathrm{tot}}} = n \cdot \frac{\pi C_{\mathrm{tot}} f_0 V^2}{Q} \tag{7}$$

where $R'_{\mathrm{tot}} = R_{\mathrm{W1}} + R_{\mathrm{W2}} + R_{\mathrm{L}}$. The increase of n scales the power stored in the clocking circuit by the same factor. Therefore the ratio of P_{RLC} and P_{RC} assumes the same expression of equation 6 and using n parallel wires does not affect the condition $Q \geq \pi$ for the quality factor of the resonating circuit.

Finally, to maintain the target resonating frequency f_0 the scaling of C_{tot} by n must be balanced by a symmetric scaling of L_{W}, therefore $L'_{\mathrm{W}} = \frac{L_{\mathrm{W}}}{n}$.

V. Evaluations

In this section we evaluate the power dissipation per unit area (P_{d} measured in $\mathrm{W/cm^2}$) of a possible layout for clock distribution. The power dissipation per square centimeter is compared to the typical limit of 100 $\mathrm{W/cm^2}$ that represents a critical limit for the capability of heat dissipation in VLSI. The considered QCA implementation is based on quantum fortresses and the dimensions involved in the computation of the parameters are summarized in figure 6. Moreover, parameters reported in table V are chosen according to the geometric rules defined in [8] and are shown in figure 7: the geometric constant $a = 220$ nm is such that each QCA cell is clocked by a single wire.

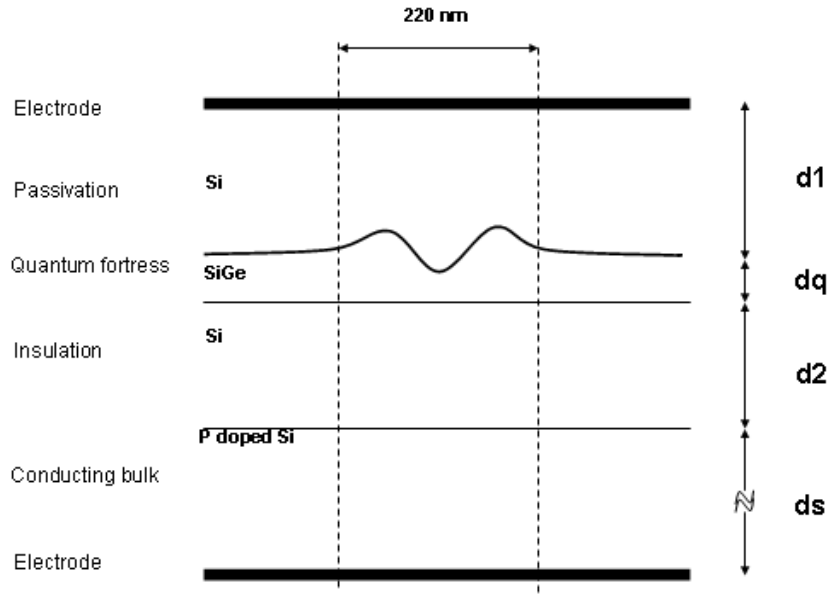

Fig. 6. Crossectional diagram of a quantum fortress type QCA chip

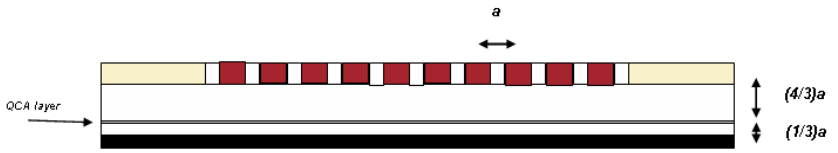

Fig. 7. Geometric constants according to [8]

First, consider the effect of the Q of the RLC resonator has on the power dissipation of the circuit for a range of frequencies (figure V). Notice that for Q=1, there is effectively no resonance, and $P_{\mathrm{RLC}} = P_{\mathrm{RC}}$. As Q increases, there is a substantial decrease in power consumption. Notice, too, that the intersection with the $100\ \mathrm{W/cm^2}$ line occurs at higher frequencies as the Q increases. Note that the plots assume that for each frequency the tuning L_{W} is set to allow resonance at that specific frequency.

The plot also shows also a Q* value of about 300 that is obtained by the given geometry and parameters reported in Table V and therefore represents the actual Q for the chosen geometries.

It is also important to look at the power dissipation for a given frequency (e.g. 1 GHz) and varying supply voltages. As can be seen in figure V, for a resonating RLC circuit with a quality factor of Q* the circuit can be driven with a voltage up to 20 V without hitting the limit of power dissipation $100\ \mathrm{W/cm^2}$. This result provides a valuable degree of flexibility since at the moment it is unknown what driving voltage will be required to obtain the switching of the quantum fortress based QCA cells from the locked to the relaxed state.

Finally we analyze the impact of the phase shift between neighboring wires on the power consumption. Figure V shows the impact of a reduced phase shift between neighboring wires given a frequency of 1 GHz and a supply

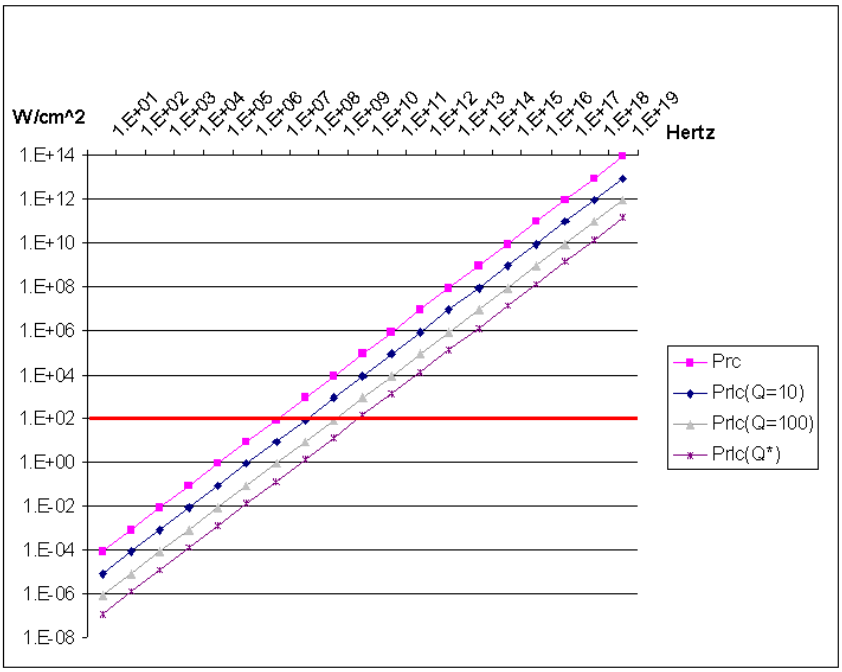

Fig. 8. P_{d} as a function of frequency for different values of Q. In red: $100 W/cm^2$ limit

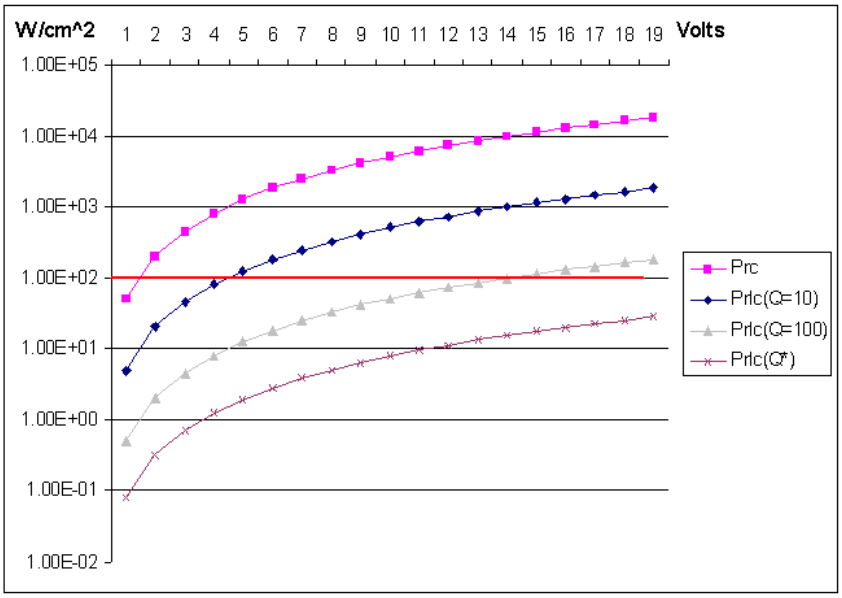

Fig. 9. P_{d} as a function of supply voltage for different values of Q at $f = 1$ GHz. In red: 100 $\mathrm{W/cm^2}$ limit

TABLE I

PHYSICAL PARAMETERS

Parameter	Value	Unit	Description
a	2.20E-07	m	geometric constant
L	1.00E-02	m	length of a wire
h	3.00E-08	m	height of a wire
w	3.00E-08	m	width of a wire
Δ	2.20E-07	m	pitch between wires
d	2.05E-07	m	distance between wires (Delta-w/2)
A_q	3.00E-10	m^2	Area facing the QCA layer
A_w	3.00E-10	m^2	Area facing the other wires
S	9.00E-16	m^2	Area of the section
ρ**(Cu)**	1.7E-08	*ohm*m*	resistivity of the wire
ρ **(Si)**	6.40E+02	*ohm*m*	resistivity of intrinsic Silicon
ρ **(P doped Si)**	1.00E-05	*ohm*m*	resistivity of P doped Silicon
ϵ_r**(SiGe)**	1.41E+01		relative permittivity of Silicon Germanium alloy
ϵ_r**(Si)**	11.68		relative permittivity of Silicon (also doped)
ϵ_0	8.85E-12	$m^{-3}kg^{-1}s^4A^2$	permittivity of free space
V_1	13	*V*	Source voltage amplitude
ϕ	1.570796	*radiant*	phase shift between adjacent wires
$d1$	2.93E-07	*m*	thickness layer 1
dq	2.44E-08	*m*	thickness QCA layer
$d2$	2.44E-08	*m*	thickness layer
ds	2.44E-08	*m*	thickness of substrate

voltage of 1 V.

From V it can be seen that for $V_1 = 1$ V the RC circuit dissipates less than $100\ \mathrm{W/cm^2}$.

Finally in figure V we analyze the effect of a reduced phase shift between neighboring wires on the power consumption for $f = 1$ GHz and $V_1 = 1$ V It can be seen with a $\phi < \pi/2$ the power dissipation can be reduced under the limit of $100\ \mathrm{W/cm^2}$ without a resonating circuit. This effect is due to the reduced capacitive load seen throughout the clocking circuitry and provides an extra parameter to reduce the power dissipation in a QCA clocking circuit when an RLC circuit is not used.

VI. CONCLUSION

This paper has addressed the characterization of the clock distribution circuits for QCA. While there is a substantial body of literature on QCA circuit design, little has been said about the clock distribution circuits required to make the QCA circuits operable. This paper has provided an electrical characterization of the parameters involved in the clocking circuitry and compared two approaches to implementing the clocking circuitry: a simple RC circuit and an improved resonating RLC circuit.

TABLE II

CIRCUIT PARAMETERS

Circuit Parameter	Value	Unit	Description
C0	8.55932E-14	*F*	Capacitance with the substrate
k(phi)	2		multiplicative factor
Cm	1.30E-14	*F*	Capacitance with adjacent wire
Ctot	1.12E-13	*F*	Total Capacitance
Rw	1.89E+05	*Ohm*	Resistance of a wire
Rl	7.30E+05	*Ohm*	Parasitic Resistance of the QCA layers
Rtot	9.19E+05	*Ohm*	Total resistance

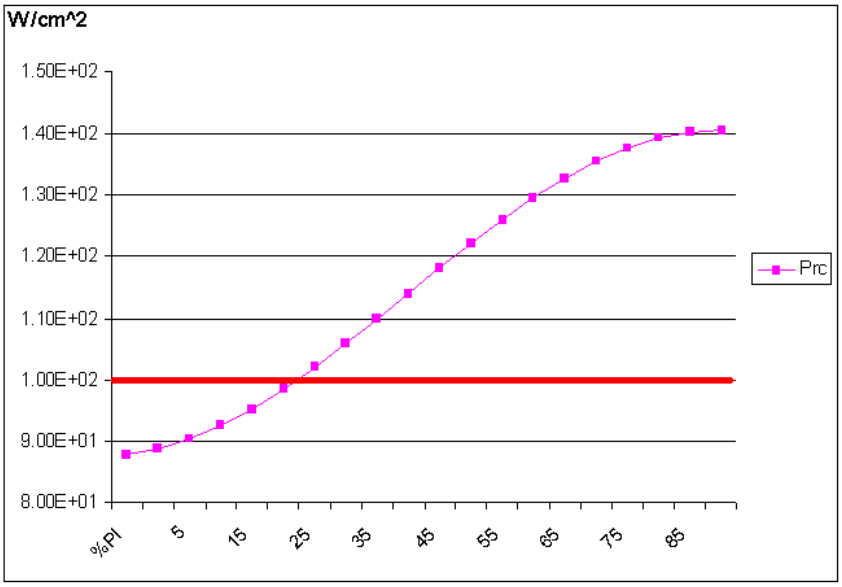

Fig. 10. P_{d} as a function of ϕ at $f = 1$ GHz and $V_1 = 1$ V. In red: 100 $\mathrm{W/cm^2}$ limit

The analysis of the RLC circuit shows that it reduces power consumption below that possible with the RC allowing the clocking circuit to operate at higher computational frequencies while dissipating less than 100 $\mathrm{W/cm^2}$.

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