New Design Principles for Cold Electronics

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***Abstract*—Josephson junctions, cryogenic CMOS, and adiabatic circuits were proposed as computing options decades ago, but never got traction due to competition from room-temperature CMOS. However, quantum computer control electronics naturally requires cryogenic temperatures, making a deeper investigation of these technologies timely.**

We argue that a technology hybrid and new system design principles are needed, which we illustrate with adiabatic cryo-CMOS circuits playing an unanticipated but very important role.

Transistor redesign will lead to even further improvement beyond what's illustrated in this paper, but more research will be needed to know how much.

Keywords—cryogenic, CMOS, cryo-CMOS, Josephson junction, RQL, quantum computer, adiabatic circuits, leakage current

I. Background

Josephson junctions (JJs), cryo-CMOS, and adiabatic circuits have been advocated for classical supercomputers due to expected 10−100× advantages in the speed-power product.

The term "supercomputer" could be used to describe the control system needed for a hypothetical scaled-up quantum computer, but the control system also has to do I/O to qubits at scalable rates like a signal processor. For popular qubits operating at 15 mK, the refrigerator's power will be at least a million times that of the electronics it cools. This factor is so extreme that it recategorizes a deeper investigation of cold electronics from "interesting" to "mission critical."

Where regular computers are a hybrid of CMOS for logic and DRAM for memory, cold electronics has two very different logic options, but the lack of a viable memory option impedes system design: JJ circuits are about 10,000× larger than equivalent cryo-CMOS circuits, but at an intermediate temperature of 4 K, cryo-CMOS consumes about 10,000× as much energy per operation.

II. Adiabatic Circuits

While cryo-CMOS is dense but runs hot, adiabatic circuits trade energy for speed. Thus, rewiring CMOS transistors into adiabatic circuits would put JJs and adiabatic transistor circuits into a similar trade space to room-temperature CMOS and DRAM. Adiabatic CMOS circuits have roughly 10× as many components as standard CMOS circuits, yet that still leaves them 1,000× smaller than the JJ equivalent.

Adiabatic CMOS circuits could thus play an important role in systems design. Most systems need more than just active logic, but the additional components can consist of memory cells, state vectors, or large amounts of logic that is not used all the time, such as row drivers in memory address decoders. Adiabatic CMOS circuits could fill these roles.

The black curves in Fig. 1 show the result of a few hundred SPICE simulations of a shift register built in a standard static CMOS logic family, versus the same function implemented in an adiabatic CMOS logic family called 2LAL,[1] all at the 180 nm node. The notable feature is that the adiabatic circuit's power dissipation decreases quadratically as clock period increases (slope −2 on the log-log graph), whereas the standard CMOS circuit's power dissipation declines only linearly (slope −1). This creates a widening energy efficiency advantage for 2LAL over standard CMOS, which ends at low frequencies due to device leakage.

The blue and red lines are analytical estimates of the same circuits using 2033, end-of-roadmap, CMOS transistors operated at 4 K. The green dot is the power in a JJ logic family called RQL running at 10 GHz.

The blue lines show typical end-of-roadmap CMOS will burn more static power than a JJ circuit running at full speed—irrespective of temperature. However, utilizing suitable CMOS transistors in adiabatic design reduces minimum power level, in principle, to that of an RQL circuit—albeit at frequencies in the low MHz range. However, there remains a lower limit on power levels due to device leakage, which needs further discussion.

III. Cryogenic Transistors

If the transistors are correctly optimized for room temperature operation, running them cold shouldn't help very much—whether the circuits are adiabatic or not. The black curves in Fig. 1 show power declining with frequency until it hits a floor set by device leakage. Total device leakage is the sum of (temperature-independent) gate leakage plus (temperature-dependent) source-drain leakage—where the two can be traded off with each other by varying gate dielectric thickness. A wise process engineer would pick a gate dielectric thickness so that the gate and source-drain leakages roughly balance at room temperature. At cryogenic temperatures, the source-drain leakage essentially goes away due to the steepened subthreshold slope, so total leakage becomes dominated by gate leakage. The unchanging gate leakage thus limits the power levels achievable in adiabatic circuits if the semiconductor process remains unchanged.

But what if the process engineer made the gate dielectric thicker than the room-temperature optimum until the gate and source-drain leakages were in balance at a lower temperature? The answer is that the total leakage would be lower.

IV. Cryogenic and Adiabatic Together

The rebalanced transistor would trade off some of the reduction in source-drain leakage due to lower temperature in exchange for lower gate leakage, yielding lower total leakage. This would extend the range of adiabatic scaling (the slope −2 range of the red line in Fig. 1) and lower the dissipation floor of the adiabatic circuit even further, provided it was operated in the MHz range.

This would allow the cryogenic adiabatic circuit to match the pW power levels of RQL gates at 1,000× higher logic density with only 200× lower logic performance. If these circuits were used in a hybrid with fast JJ circuits, the slower speed would not be limiting at the system level.

Deliberately designing transistors for extremely low leakage at cryogenic temperatures might enable two other important usage scenarios, but ultimate limits to low leakage are not yet known:

- A dense, high-speed adiabatic CMOS memory about 1% as fast as RQL logic. (Note microprocessors and DRAM function properly with a 100:1 speed ratio.)
- Effective transistor operation even below 4 K, making transistors a viable option if necessary to support a very cold qubit or sensor element.

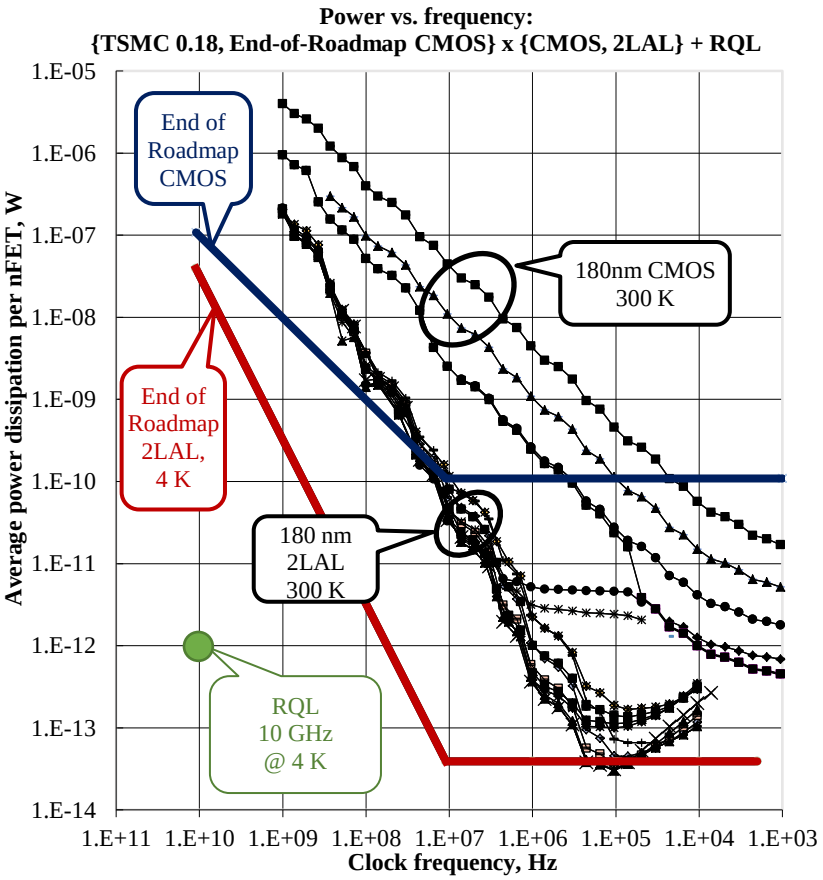

Fig. 1. The black curves plot of a few hundred SPICE simulations of standard CMOS and 2LAL, a different circuit made from the same transistors. The gap between the two circuits increases as clock rate declines. CMOS (blue) always dissipates more power than a JJ circuit called RQL, but adiabatic 2LAL may dissipate less at low speed. The 2LAL and RQL curves do not include cooling overhead, which is consistent with the conclusions of this document.

V. Conclusions

We presented cryogenic adiabatic CMOS circuits to illustrate system-level design for electronics that spans a range of temperatures.

Adiabatic CMOS does not break new ground viewed in isolation, because JJs are faster and lower power, while standard CMOS is denser. However, making all three options available to the designer will allow him or her more flexibility to create a faster, lower power, and more cost-effective system.

The ideas in this short paper also suggest device physics research into low-leakage transistors at cryogenic temperatures. There are IoT transistors now in production with leakage less than 1 pA at room temperature, but achieving 1 aA (10^{-18} A, or ~6 electrons/sec) at 4 K would make cryogenic memory more effective. A stretch goal might be a transistor that could be co-located with qubits in the 15 mK stage of a quantum computer, which might require less than 1 leaking electron per second.

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