Semi-Automated Design of Functional Elements for a New Approach to Digital Superconducting Electronics

Methodology and Preliminary Results

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***Abstract*— In an ongoing project at Sandia National Laboratories, we are attempting to develop a novel style of superconducting digital processing, based on a new model of reversible computation called Asynchronous Ballistic Reversible Computing (ABRC). We envision an approach in which polarized fluxons scatter elastically from near-lossless functional components, reversibly updating the local digital state of the circuit, while dissipating only a small fraction of the input fluxon energy. This approach to superconducting digital computation is sufficiently unconventional that an appropriate methodology for hand-design of such circuits is not immediately obvious. To gain insight into the design principles that are applicable in this new domain, we are creating a software tool to automatically enumerate possible topologies of reactive, undamped Josephson junction circuits, and sweep the parameter space of each circuit searching for designs exhibiting desired dynamical behaviors. But first, we identified by hand a circuit implementing the simplest possible nontrivial ABRC functional behavior with bits encoded as conserved polarized fluxons, namely, a one-bit reversible memory cell with one bidirectional I/O port. We expect the tool to be useful for designing more complex circuits.**

Keywords—Superconducting logic; long Josephson junctions; flux solitons; reversible computing; elastic fluxon interactions

I. INTRODUCTION

Whenever there is a goal of improving aggregate computational performance within any power-limited application scenario, the most general way to achieve this is if the computational energy efficiency (useful operations performed per unit energy dissipated) of the underlying information processing technologies (including logic, memory, and communication functions) is improved as well. Typically, when manufacturing cost is a concern, we wish to improve the energy efficiency of the technology at any given cost-efficiency design point (defined as aggregate performance per unit manufacturing cost).

This goal then raises a serious challenge for any long-term strategic plan for innovation in future computing technologies, specifically, to identify a sustainable trajectory for continuing to improve computational energy efficiency that also minimizes any negative impacts on manufacturing cost-efficiency.

The existing design styles for superconducting logic fall primarily into two classes, neither of which offers a prospect that can clearly be maintained in the long term for continually improving energy efficiency at a given level of cost-efficiency:

- *Irreversible SFQ-based logics*, such as RSFQ [1], ERSFQ [2], eSFQ [3], RQL [4], *etc.* encode and transmit information in single flux quanta (SFQ), but manipulate these in a logically and physically irreversible manner, dissipating at least on the order of the SFQ energy with each logic operation. Meanwhile, the SFQ energy, itself, is constrained by reliability requirements to be relatively large compared to the kT thermal energy scale, typically on the order of 100 kT or larger. Thus, for any given environment temperature T, there is no long-term potential to continue improving the energy efficiency of these logic styles over many more orders of magnitude.
- *Adiabatic superconducting logics*, such as AQFP/RQFP [5][6], Ren & Semenov's nSQUID approach [7], and the classic parametric quantron style of Likharev [8] can theoretically approach unlimited energy efficiency, but at the cost of reduced operating frequency; this then also reduces manufacturing cost-efficiency for attaining given parallel throughput. Thus, at any fixed target level of cost-efficiency, this approach does not provide a path to continue improving energy efficiency within a cost-efficiency constraint, if we assume that the manufacturing cost per logic gate cannot decline indefinitely.

Can we perhaps identify a *new* path forwards for superconducting logic that may avoid the limitations inherent to the above two categories of approaches? Such a logic style would need to have the following properties:

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- Like the methods described in [6]–[8], it should approach *logical and physical reversibility*, reusing the digital signal energy for multiple useful operations while dissipating only an arbitrarily-small fraction of the signal energy on each operation;
- However, beyond this, it should not be inherently limited by the fixed energy-delay products of the existing *adiabatic* styles of reversible superconducting logic, but should permit steady increases in energy efficiency without correspondingly substantial reductions in manufacturing cost-efficiency (performance per device).

Could such a *super-reversible* superconducting logic style exist? A realistic hope that this question may ultimately be answered in the affirmative is provided by the existence of *superadiabatic* processes in physics, going back to the study of Landau-Zener transitions in scattering processes [9][10]. The general lesson here is that, in suitably-organized interactions between quantum systems, the parasitic excitation induced by the interaction, which must ultimately be dissipated, scales down *exponentially* with the (transition time proportional) adiabaticity parameter, rather than linearly, as would be the case in classical adiabatic processes. This then suggests that reversible computational processes that exhibit arbitrarily small energy-delay products are in fact possible, and moreover, the potential for this was recently demonstrated more concretely in the context of quantum-dot cellular automata (QDCA) [11]. Furthermore, in recent years, physicists have also explored the theory and applications of an even broader variety of so-called *shortcuts to adiabaticity* (STA) [12] which may be useful.

To access an enhanced superadiabatic scaling of dissipation in a superconducting context, we wish to get away from the traditional physical computing mechanisms utilized in the existing adiabatic superconducting logics, and explore a *new* type of reversible superconducting logic, such as, for example, ones that might be made more closely reminiscent of the types of scattering processes that can benefit from leveraging the Landau-Zener formula. Specifically, in this work, we wish to consider a new logic style based on ballistic propagation of single flux quanta (SFQ) between interaction points at which they deterministically *scatter elastically* (or as nearly so as can be arranged). A major challenge in any such scheme is suppressing the tendency towards chaotic instability, which often tends to be an endemic characteristic of nonlinear conservative dynamical systems. Two ideas that, in combination, we are currently exploring for suppressing the tendency towards chaos in the context of a ballistic-elastic SFQ computing technology are:

- Utilize discrete *topological* degrees of freedom, which naturally tend to be stable and self-restoring to digitally well-defined states in the face of small perturbations. An example of such a topological quantity in a superconducting circuit would be the presence of a flux soliton or *kink* (also just called a *fluxon*) in a *long Josephson junction* (LJJ) style transmission line. A fluxon in an LJJ can be considered to effectively constitute a type of topological soliton, which conserves the orientation of the quantized flux toroid that is threaded through and around a localized segment of the (spatially-extended) junction. These topological states are *naturally stable* entities (retaining their cohesiveness indefinitely), except that they can mutually annihilate when two oppositely-polarized fluxons encounter each other.
- More generally, we not only want to avoid the (clearly dissipative) annihilation events, but also *any* direct interactions between moving fluxons, since in general these would tend to allow any uncertainties in the relative timing of the fluxons to be amplified exponentially, leading to chaotic instabilities in the overall dynamics of the system. However, note that direct interactions can be avoided if different fluxons encounter designated interaction sites at *widely separated* points in time, and if the dynamical state of the circuit at the interaction site can be treated as having relaxed into a locally stationary state by the time of the next fluxon's arrival.

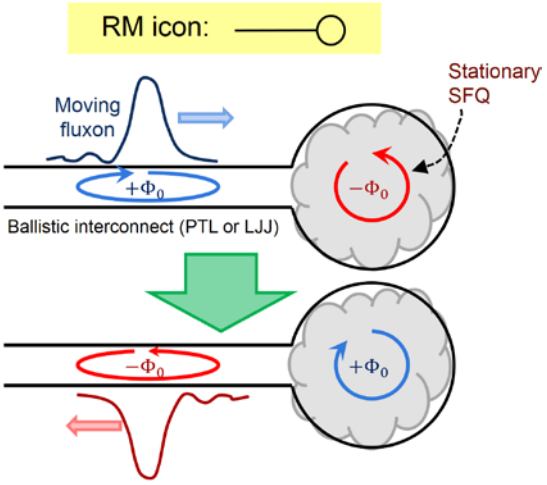

Fig. 1. Abstract sketch of a broad family of design concepts for a subcircuit implementing the *Reversible Memory* (RM) behavioral functionality. A planar, unbiased, reactive circuit (cloud) with a continuous superconducting boundary conserves flux and roughly conserves energy if all JJs always (or almost always) remain subcritical. The functional goal for this circuit is that a flux soliton with suitable velocity arriving ballistically on an LJJ should *elastically scatter* from the interaction circuit, while exchanging flux polarity with the trapped SFQ. One (very preliminary, but functional) initial hand-design for such a circuit is shown in Fig. 2.

The appropriate general abstract model of digital computation that corresponds to the physical requirements envisioned above, which we call Asynchronous Ballistic Reversible Computing (ABRC), was previously worked out by M. Frank [13], and in a more recent paper [14], we began exploring fluxon propagation in LJJs, and identified the simplest useful functional element in the ABRC class that conserves total oriented flux while utilizing flux polarization to encode binary data: This is a one-port, two-state behavioral primitive which we call the *reversible memory* (RM) cell (Fig. 1); its digital function is simply that a fluxon impinging on its single I/O port re-emerges, but with its polarization swapped with that of a stationary SFQ-containing element within the device (Table I). Considered as a memory cell, this device operation is reading out the old bit-value and writing in a new bit-value simultaneously, in a logically and also (almost) physically reversible manner.

TABLE I. TRANSITION TABLE FOR THE DIGITAL FUNCTIONAL BEHAVIOR OF THE REVERSIBLE MEMORY (RM) ELEMENT

Input Syndrome		**Output Syndrome**	
Incoming Fluxon Polarity	***Initial Stored Fluxoid No.***	***Final Stored Fluxoid No.***	***Outgoing Fluxon Polarity***
+1	(+1)	(+1)	+1
+1	(−1)	(+1)	−1
−1	(+1)	(−1)	+1
−1	(−1)	(−1)	−1

The immediate challenge motivating the present work is to design a superconducting circuit that actually implements the RM functionality in an energy-efficient manner, with minimal energy loss from the soliton mode. We also wish to identify implementations of additional ABRC circuit elements, leading up to a full universal set of primitives. The vision here is that input fluxons could be introduced into a complex ABRC circuit, shuttle around elastically within the structure, and emerge from the circuit in a configuration that encodes the result of multiple parallel and sequential steps of computation, with the majority of the initial fluxon kinetic energy still present, and with minimal dissipative losses.

An even longer-term vision here is that, if we can leverage the advantageous scaling of superadiabatic processes, then the degree of elasticity of the fluxon-device interactions might be continuously improved as the technology is further refined without incurring significant device slowdowns, creating a long-term development path towards increasing the energy-efficiency of superconducting logic at fixed cost-efficiency, a path which does not currently exist.

The most closely-related research to the effort pursued here is the work by Osborn and colleagues at the University of Maryland (*e.g.*, *c.f.* [15]), who are also investigating a ballistic fluxon-based logic. The primary distinction between their approach and ours is that, so far, they have been focusing (for the case of elements with multiple inputs) on synchronous, stateless reversible gates such as CNOT, whereas we predict that the use of asynchronous, stateful elements, such as are contemplated in the ABRC model, will ultimately be required in order to achieve the maximum possible levels of energy efficiency.

II. REVERSIBLE MEMORY CELL IMPLEMENTATION

During the period leading up to the ISEC 2019 conference, after an *ad hoc* process of manual design-space exploration, we identified a simple circuit (Fig. 2) that successfully implements the desired digital functional behavior for the RM while also preserving (in the output flux soliton mode) the majority of the energy of input fluxons within a certain range of energies (which remains to be fully characterized). This RM circuit was tested using the same test bench setup (Fig. 3) that we used in [14] (in which the circuit under test was just a terminating resistor). WRSPICE simulation results for positively-oriented input fluxons and two different values ($\pm\Phi_0$) of the initially-stored fluxoid are shown in Fig. 4. Note that in both cases, the circuit successfully executes a digital exchange of quantized flux. Due to the time reversal invariance of electrodynamics (ignoring weak interactions), the results obtained imply that the circuit's functional behavior for negatively-signed input fluxons is also correct (since these cases just have the momentum vectors of all charge carriers reversed).

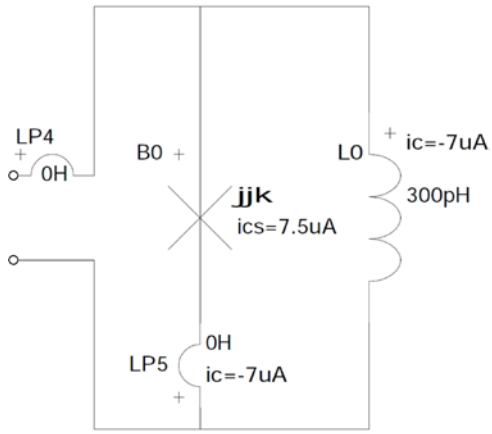

Fig. 2. Schematic captured in XIC for a minimalistic implementation of the RM cell concept from Fig. 1. The junction is sized to have a critical current of I_c = 7.5μA which is roughly half the peak current of the input fluxons in our test environment (Fig. 3). The inductance of the storage loop is sized to a value of L = 300 pH which allows it to contain just ±1 flux quantum, and in this example, the flux threading the loop is initialized using `ic` (initial condition) device parameters to about −1 flux quantum. Initially, a current of I = 7 μA ≈ 6.89 μA ≅ Φ_0/L is circulating counter-clockwise in the loop; the closest permitted value of the quantized fluxoid is then exactly $-\Phi_0$. This design works in our test setup; example traces are shown in Fig. 4.

Although this particular circuit works in simulation, as far as its digital behavior is concerned, it is only a very preliminary first step towards eventually attaining a complete ABRC design discipline, and much work remains to be done. For example:

1. We need to more comprehensively understand, and at a

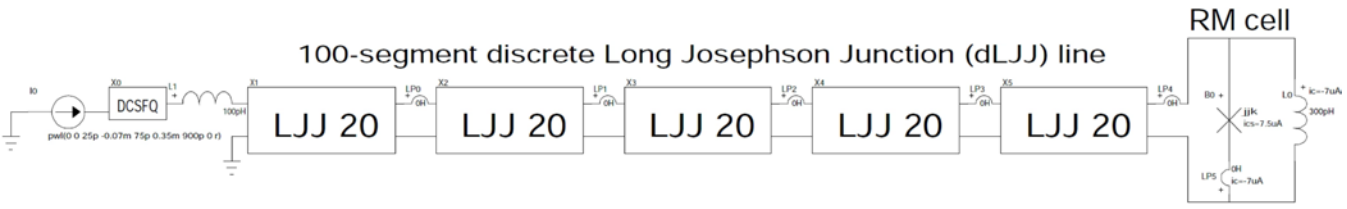

Fig. 3. XIC schematic for test bench for exercising the RM cell from Fig. 2. The 100-JJ discretized LJJ interconnect is identical to the one from Fig. 3 of [14], except here shown broken into 5 segments of 20 cells each, for purposes of inserting probe points. The SFQ pulse source at the left (a DC-to-SFQ converter driven by a piecewise-linear current source, with a 100 pH inductor for pulse spreading) is also identical to the one in [14]. The circuit under test at the right is the RM cell from Fig. 2 above. Example traces for this design (for two different initial values of the loop current) are shown in Fig. 4.

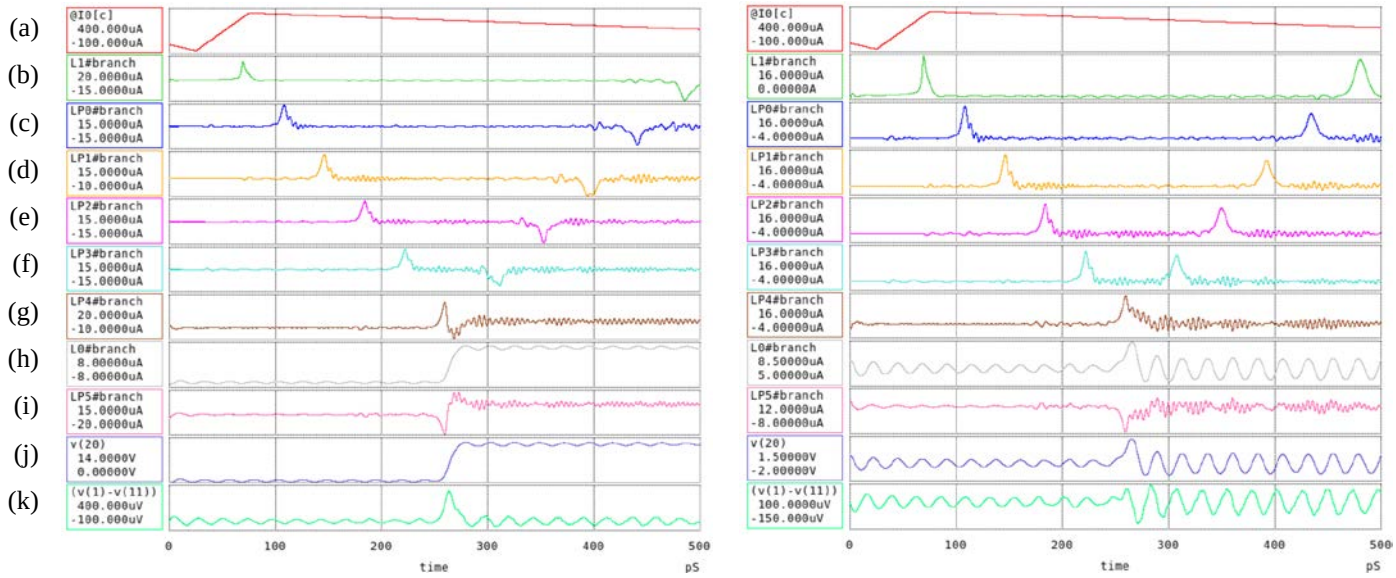

Fig. 4. Traces from WRSPICE simulation of the test bench in Fig. 3 for two different values of the initial fluxoid quantum number in the storage loop (−1 and +1, respectively). From top to bottom, traces are: (a) Current source I0; (b) current on input inductor L1; (c)–(g) currents on dummy probe inductors LP0–LP4; (h) current on storage inductor L0; (i) current through JJ (B0); (j) accumulated phase across JJ ("V"=proxy for radians) and (k) voltage across JJ. In both cases, traces (b)–(g) show the positively-oriented input flux soliton approaching the storage loop, at which point, one of two things happens: (Left) If the stored fluxoid value has opposite sign to the input fluxon, note the current on the storage loop inductor (h) changes sign (from approx. −6 μA to +6 μA), while the junction phase (j) accumulates $+4\pi \approx +12.6$ and a net $+2\Phi_0$ of flux (k) crosses the junction towards the right (since a positive fluxon moves into the loop, and 1 negative fluxon moves out), and note, the fluxon emitted backwards along the dLJJ has negative polarity. (Right), If the stored fluxoid polarity *does* match that of the input fluxon, note that the reflected fluxon retains unchanged polarity, and the average loop current and junction phase remain unchanged, so there is no net flux transfer. Either case can be described as an exchange of flux orientation between the moving and stationary SFQs, so the circuit's digital behavior is correct. The major oscillations in the last four traces are an artifact of the artificial initial non-equilibrium flux distribution in the vicinity of the storage loop, and can be gradually damped out if needed before operation.

more abstract theoretical level, what exactly are the engineering requirements for this circuit to work properly, and why. We then need to explore whether that understanding can be generalized to apply to the case of more complex digital behaviors for ABRC functional elements.

2. We also need to characterize the operating margins for this circuit, that is, determine the region of the design parameter space over which the digital behavior of the circuit remains correct.

3. At the moment, the circuit's operation does not in fact preserve 100% of the input fluxon energy in the outgoing flux soliton mode; this can already be seen by inspection of the traces in Fig. 4 (note that the outgoing fluxons are wider than the incoming ones; they are also approximately 15% slower, reflecting a reduced kinetic energy). Thus, the interaction is not completely elastic. This is not surprising since, during operation, there will be a certain amount of dissipative quasiparticle current flowing across a voltage drop while the junction phase is transitioning. However, these losses may be reduced through further refinement of the design. We still need to explore how the energy conservation efficiency (*i.e.*, the degree of physical reversibility, or elasticity) of this circuit varies as a function of the circuit parameters and the input fluxon energy.

4. We also need to explore whether a more elaborately designed version of the circuit might achieve a higher value of the peak energy efficiency. Also, the elasticity of the device operation might be improved by utilizing different materials or operating at lower temperature, such that the quasiparticle density is lower.

In any case, even at this very preliminary stage, the discovery of a working RM cell design is valuable, because (a) it validates that ABRC's core concept, of informationally nontrivial, logically reversible and mostly-elastic interactions between ballistic and stationary state-bearing entities, really does make sense physically, and (b) it gives us a starting point which can serve as a useful reference for the further exploration of the design space for implementation of this and other ABRC functions.

III. Design-Space Exploration Methodology

To help us more quickly find improved implementations of the RM functionality, as well as implementations of more complex ABRC element functionalities, we are in the process of developing a methodology for carrying out semi-automatic, systematic exploration of the design space.

A. Design Constraints

We have identified a number of *a priori* design constraints that will be applied to the family of circuit designs that we will initially consider in this study. However, if no suitable circuits are found that satisfy all of these constraints, some of these constraints may be loosened as needed, while continuing to search for the least-dissipative available solutions.

- The circuit may *not* include any elements with nonzero, finite DC resistances, but only pure reactive elements, *i.e.*, those featuring divergent DC resistance or conductance, such as (among linear elements) superconducting inductors, lossless capacitors and mutual inductances between superconductors.
- Initially, the only nonlinear element considered will be undamped (*i.e.*, not self-shunted) Josephson junctions (JJs), although other types of superconducting devices such as quantum phase-slip junctions or magnetically biased JJs may also be considered in the future;
- Further, the design should be such that any JJs that exist in the circuit should spend little or no time in the supercritical voltage state ($I > I_c$), minimizing the dissipative impact of the junction's normal-mode resistance R_N;
- And further, minimal time should be spent on the subgap (quasiparticle) branch as well, and/or the subgap resistance R_0 should be large, to minimize V^2/R_0 losses.
- Initially, we will consider only circuit designs that can be rendered as planar schematics with a continuous superconducting boundary (*i.e.*, no JJs or capacitors on the boundary), since such circuits must conserve total flux threading the boundary. This constraint simplifies the design space, but it is rather arbitrary, and can be loosened if necessary.
- Initially, we will consider only circuits with *no* bias currents (neither DC or AC), since our goal is to approach a design that requires no power input besides the initially injected data fluxons. But in practice, applications of our technology will likely provide some power in bias lines to continually compensate for the actual (but still very small) losses that will exist in the circuit.
- Care should also be taken in the detailed physical realization of the circuit to minimize parasitic dissipative effects resulting from RF emission, loss tangents in surrounding dielectric materials, and other physical nonidealities. However, our initial investigations will be carried out at the electrical schematic level only, and will therefore ignore such effects.

B. *Circuit Search Methodology*

Because our proposed concept for how to carry out digital computation in superconducting circuits is completely new, an effective methodology for hand-design of these circuits is not immediately obvious. Many of the established practices of SFQ-based circuit design, such as those utilized in RSFQ and related logic styles, simply are no longer applicable when one is aiming for a nondissipative design. We suspect that successful design methodologies within our domain may utilize analytical techniques such as matching of timescales, *e.g.* between those of the input flux pulse duration, and the natural timescales for the relevant dynamical transitions within the stateful circuit at the scattering center. General RF design techniques such as impedance matching may also be useful. In addition, more advanced theoretical tools such as S-matrix scattering theory and/or perturbation analysis could conceivably also be fruitfully brought to bear on our design problem.

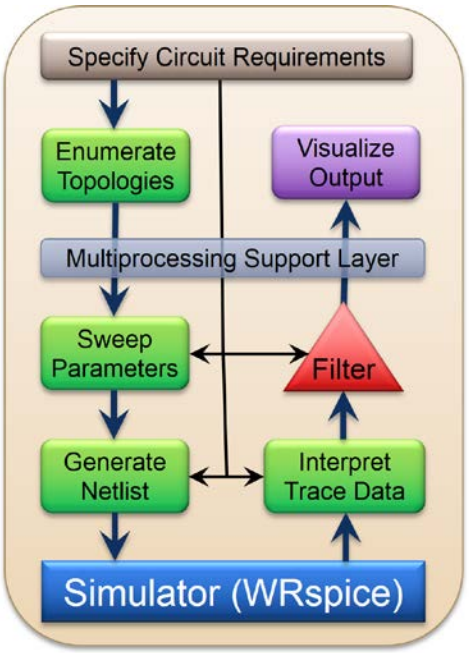

Fig. 5. Sketch of the software architecture for SCIT, the Superconducting Circuit Innovation Tool. See discussion in Sec. III.B.

However, in the interim, while appropriate theoretical tools are still being investigated, we can already make some headway by carrying out an automated search through design space to identify working circuits. To this end, we are implementing a software system called SCIT, the Superconducting Circuit Innovation Tool. A sketch of our initial software architecture concept for SCIT is shown in Fig. 5. In outline, the overall processing workflow to be carried out in SCIT is as follows:

1. Accept as input a formally-specified definition of the requirements for the circuit design;
2. Enumerate possible circuit topologies, in order of increasing complexity, up to some maximum number of primitive circuit elements;
3. Delegate topologies to nodes in a multiprocessing cluster to analyze;
4. For each topology, sweep across (or do Monte Carlo sampling of) the joint device parameter space of the circuit;
5. Generate a WRSPICE netlist for each candidate circuit design;
6. Run WRSPICE to simulate the circuit operation;
7. Automatically summarize and interpret the resulting traces to assess pass/fail criteria (*e.g.*, did a fluxon of desired polarity emerge on a specified LJJ interconnect within a specified time window?) and figures of merit (*e.g.*, what fraction of the input fluxon energy is contained in the output fluxon)?

8. Filter output for results that meet some desired threshold for reporting purposes;
9. Facilitate automated visualization (e.g., schematic capture) of successful or otherwise-interesting designs.

The initial implementation of SCIT is being developed in the Python (3.x) programming language.

IV. CONCLUSION

In this ambitious line of work, we are attempting to establish the foundations of a new technology base, and blaze a new trail towards a more sustainable path for long-term improvements in the energy efficiency (at given levels of cost-efficiency) of superconductor-based approaches to digital computation.

In this paper, we reviewed the motivation for our new *asynchronous ballistic* reversible approach to digital computation in superconducting electronics, presented an example Josephson junction circuit that implements one of the digital functions in our model, and outlined the computer-assisted methodology that we are pursuing to help us systematically uncover more sophisticated circuit designs for more complex functions.

Of course, there is a large amount of work that remains to be done in this new line of research. We look forward to continuing to make progress in this effort over the coming years.

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