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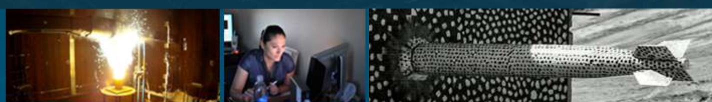
Improved superconducting logic families — (asynchronous, ballistic, reversible, *etc.*) a difficult engineering challenge for SCE



PRESENTED BY

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Challenge: Design improved superconducting logic families

Examples of some desirable qualities for a new logic family:

- Further ***increased computational energy efficiency***…
  - Note: *As a function of* the logic propagation delay!
    - An important cost metric to minimize for applications: Energy-delay product (EDP)
    - Research challenge question: Is it possible to closely approach the ideal of *reversible* operation while maintaining reasonable performance?
      - There are known fundamental quantum lower limits on *signal energy* (× delay), but *not* on energy *dissipation* (× delay) for performing logically-reversible operations
- ***Reduced logic gate complexity*** (and fab cost), including *fully-routed* area per gate
  - Clock & bias networks introduce substantial overhead in circuit complexity
  - Can we design gates that support *unclocked* operation (or reduced clocking)?
  - Could we even design gates that require *no bias current supply*?
    - *I.e.*, that operate using the energy of the input logic signal (*e.g.*, fluxon) alone?
- ***Improved noise margins***
  - Reduced sensitivity to various dimensions of variability (process, fields, temperature, *etc.*)
  - More robust functional behavior (fewer/rarer gate failure modes)

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Why is this important?

Table CEQIP-4 Common Superconductor Digital Logic Families

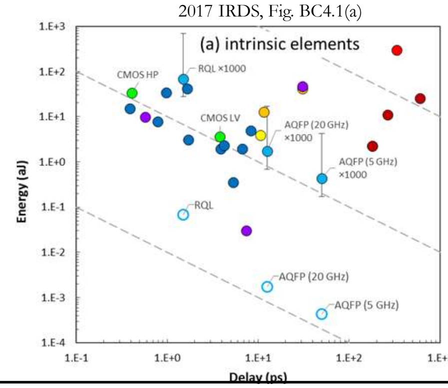
Name	References	Power	Static Power	Dynamic power (per JJ)	Trans-formers	Static Gates
RSFQ: rapid single flux quantum	[38]	DC	High	$\alpha I_c \Phi_0 f$	No	No
LR-RSFQ: inductor-resistor RSFQ	[39, 40]	DC	Low	$\alpha I_c \Phi_0 f$	No	No
LV-RSFQ: low-voltage RSFQ	[41, 42]	DC	Low	$\alpha I_c \Phi_0 f$	No	No
ERSFQ: energy-efficient RSFQ	[43, 44]	DC	0 *	$I_b \Phi_0 f$	No	No
eSFQ: energy-efficient SFQ	[45, 46]	DC	0 *	$I_b \Phi_0 f$	No	No
DSFQ: dynamic SFQ	[47]	DC			No	Some
RQL: reciprocal quantum logic	[48, 49, 50]	AC	~0	$\alpha I_c \Phi_0 f\, 2/3$	Yes	Some
PML: phase mode logic	[51]	AC	~0	$\alpha I_c \Phi_0 f /3$	Yes	Some
AQFP: adiabatic quantum flux parametron	[52]	AC	~0	$\alpha I_c \Phi_0\, 2\, \tau_{sw} / \tau_x$	Yes	No

(From draft IRDS chapter on Cryogenic Electronics & Quantum Information Processing)

Of course, there are already a substantial number of fairly well-developed superconducting logic families that exist already, such as these →

- However, they have limitations:
  - **Noise margins** are still often not as large as would be desirable
    - Excessive sensitivity to trapped flux, process variations, local heating…
  - **Energy efficiency *is still not competitive*** for systems operating within room-temperature external environments
    - When taking into account specific power of the cryo-cooling system →
      - Applying reversible computing principles may be *required* to do much better
  - Usually require fully (or mostly) ***synchronous* operation**
    - All (or most) logic gates must be clocked
      - Incurs substantial overhead to route clocks to all gates

2017 IRDS, Fig. BC4.1(a)



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Asynchronous Ballistic Reversible Fluxon Logic

A general concept for a new class of superconducting logic families

- Presently under development at Sandia
  - 3-year project, funded by a $1.5M internal grant

A fully-general asynchronous circuit model of reversible computing, called *Asynchronous Ballistic Reversible Computing* (ABRC) was already formulated last year

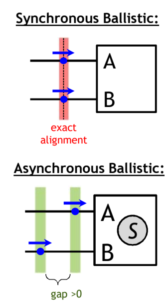
- Presented at the IEEE Int'l. Conf. on Rebooting Computing (ICRC 2017)

This year (1st year of project), we began exploring how to implement special cases of the general ABRC model in ballistic fluxon-based logic

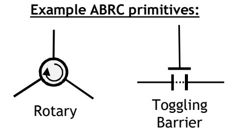
- Looking at discretized Long Josephson Junctions (LJJs) for ballistic interconnects
  - Fluxon velocity is low, but stability of soliton mode facilitates initial explorations
- Beginning to characterize the set of ABRC functions that consistent with conservation & symmetry constraints that apply in reactive JJ circuits

Next steps:

- Design circuits implementing useful ABRC functions, optimize energy efficiency

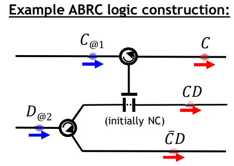


Example ABRC primitives:



(First set of ABRC primitives proved to be computation universal)

Example ABRC logic construction:



(AND from toggling switch gate)

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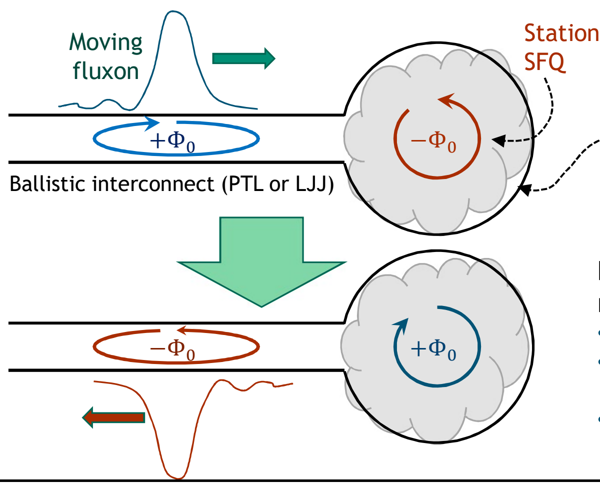
An example "baby step" towards inventing a better SC logic family…

The below is in the nature of a small, concrete research challenge problem:

- As a community, can we solve the following superconducting circuit design exercise?
  - Either find a solution, or prove *rigorously* that it's impossible under the given constraints



Problem: *Design a Ballistic Reversible Memory Cell*

Some planar, reactive SCE circuit with a continuous superconducting boundary (to be designed)

- *Only* contains L's, M's, C's, and *unshunted* JJs
- Conserves total flux, ideally nondissipative

Desired circuit behavor (NOTE: conserves flux, respects T symmetry & logical reversibility):

- If polarities are opposite, they are swapped (shown)
- If polarities are identical, input fluxon reflects back out with no change in polarity (not shown)
- *Elastic scattering* type interaction: Fluxon kinetic energy is (almost entirely) preserved